

WHAT IS CLAIMED IS:

1. A CMOS image sensor, comprising:

a substrate;

a photodiode sensory region located in the substrate;

5 a transistor device region located in the substrate, wherein the photodiode sensory region is isolated from the transistor device region by an isolation layer;

a transistor located on the transistor device region, wherein the transistor comprises a gate oxide layer, a gate conductive layer, a spacer and a source/drain region;

a self-aligned block, located on the photodiode sensory region; and

10 a protective layer located on the substrate, covering at least the self-aligned block.

2. The CMOS image sensor of claim 1, wherein the protective layer includes a material that prevents erosion from plasma etching.

15 3. The CMOS image sensor of claim 1, wherein the protective layer includes silicon nitride.

4. The CMOS image sensor of claim 1, wherein the self-aligned block includes silicon oxide.

20 5. The CMOS image sensor of claim 1, wherein the self-aligned sensory region includes a doped region and a dopant type for the doped region is same as that for the source/drain region.

6. The CMOS image sensor of claim 1, wherein the CMOS image sensor further includes a silicide layer to cover the gate conductive layer and the source/drain region.

7. The CMOS image sensor of claim 1, wherein the substrate comprises a p-type dopant and the photodiode sensory region comprises an n-type doped region.

8. The CMOS image sensor of claim 1, wherein the substrate comprises an n-type dopant and the photodiode sensory region comprises a p-type doped region.

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